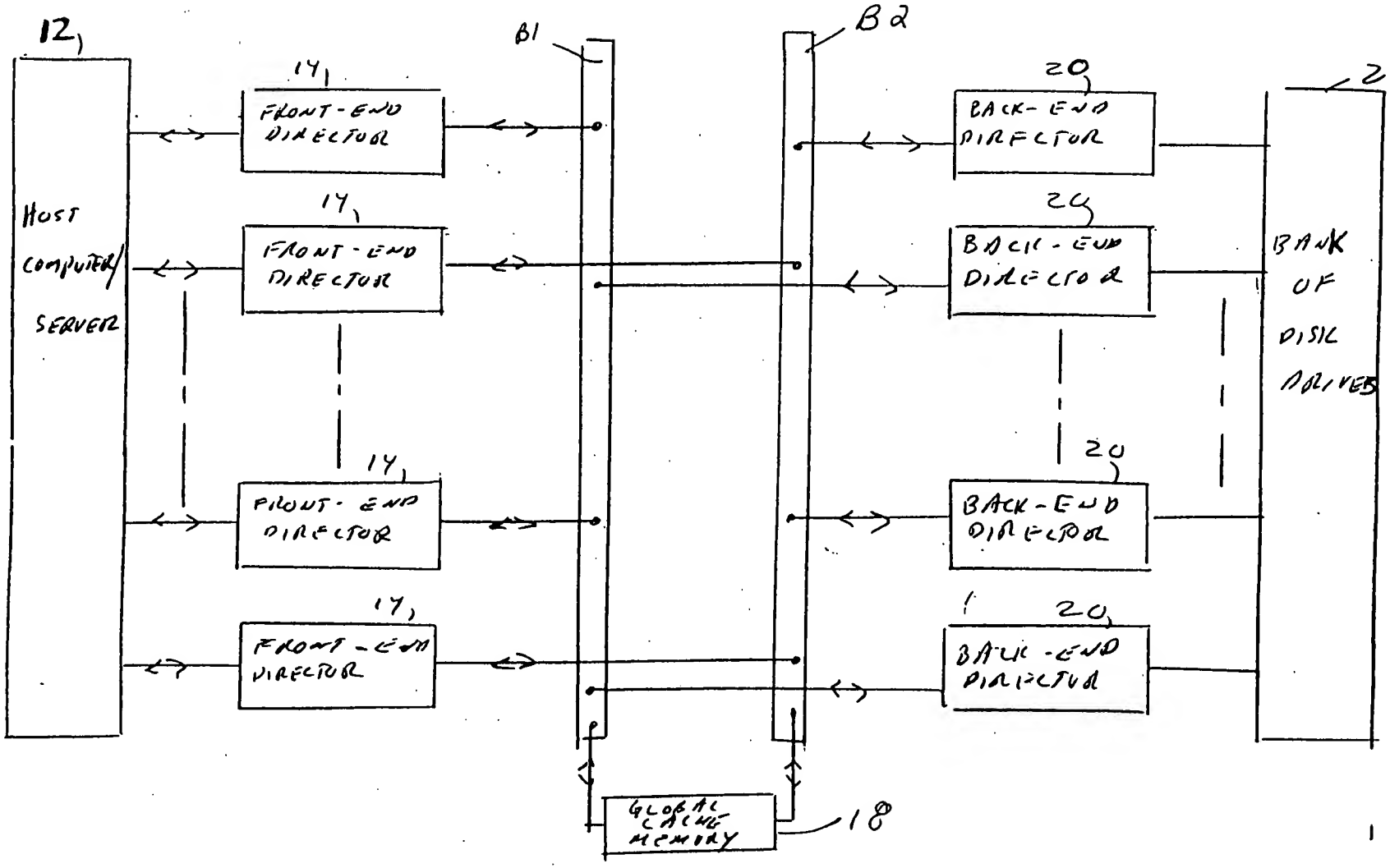
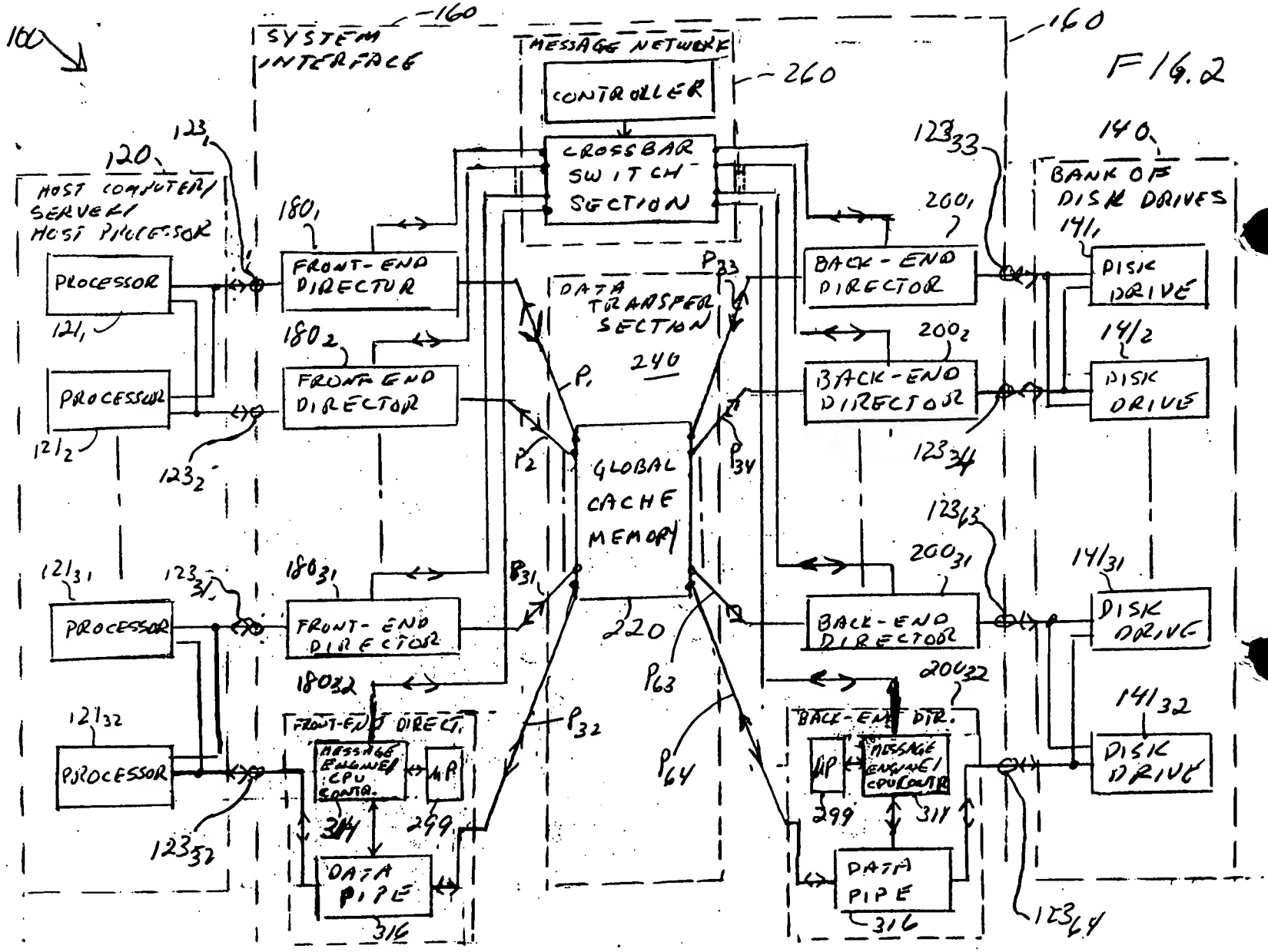
DOCKET 99662560

FIG. 1
PRIOR ART



DOCKET 95-95-950



F16.2

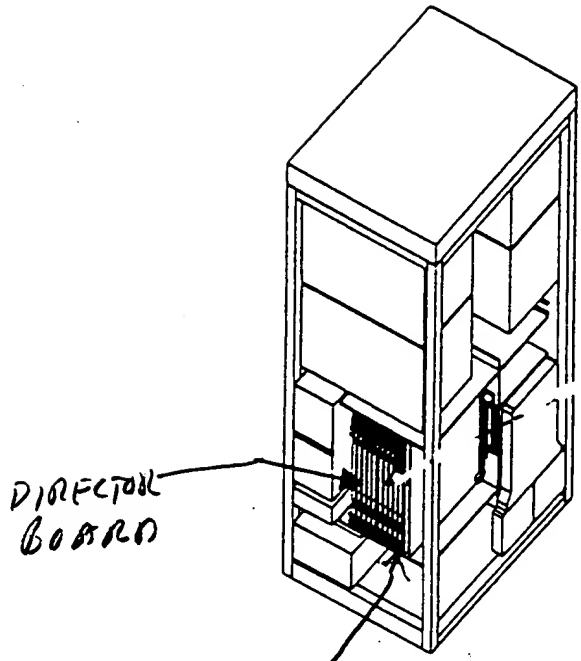
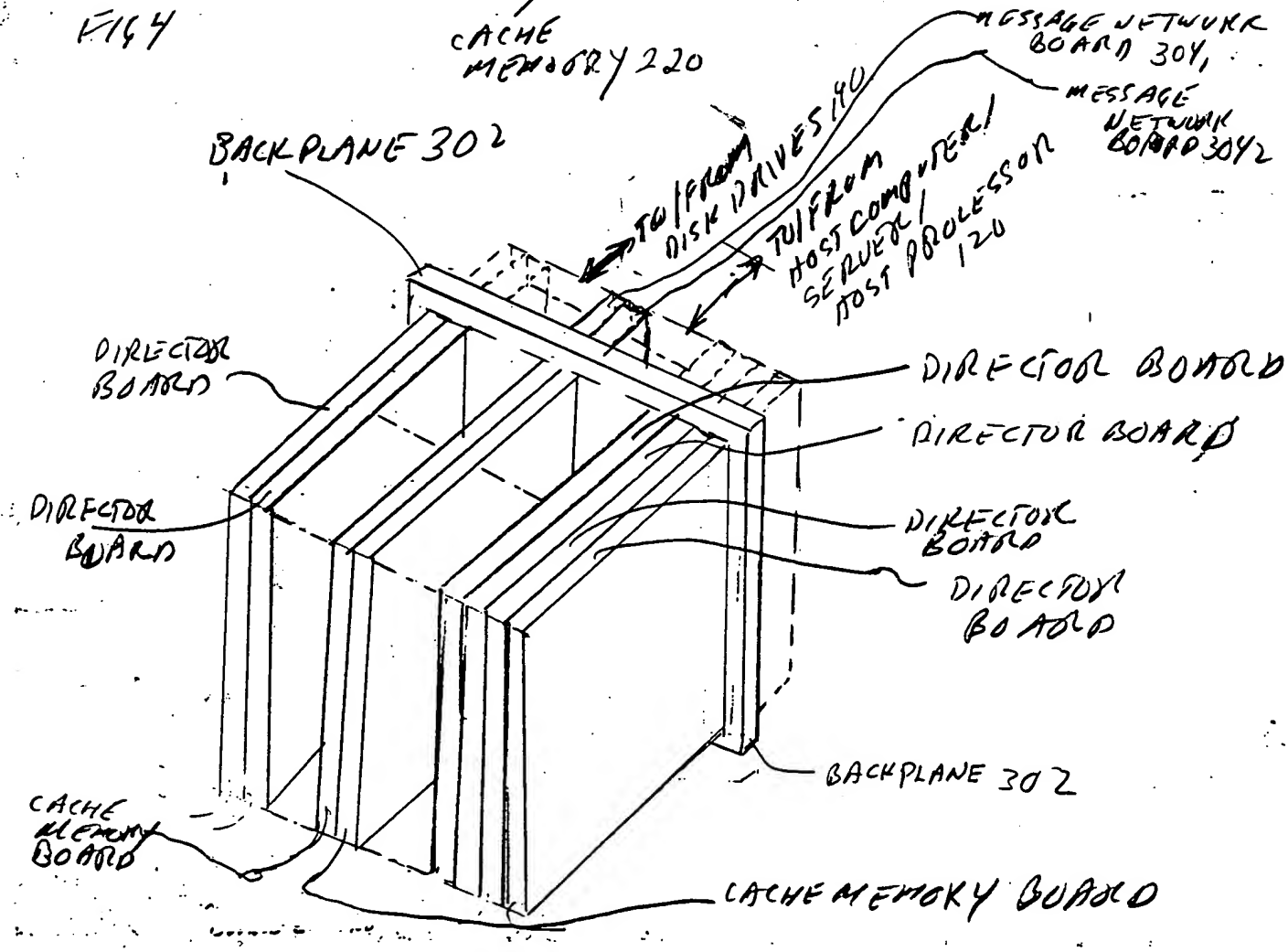
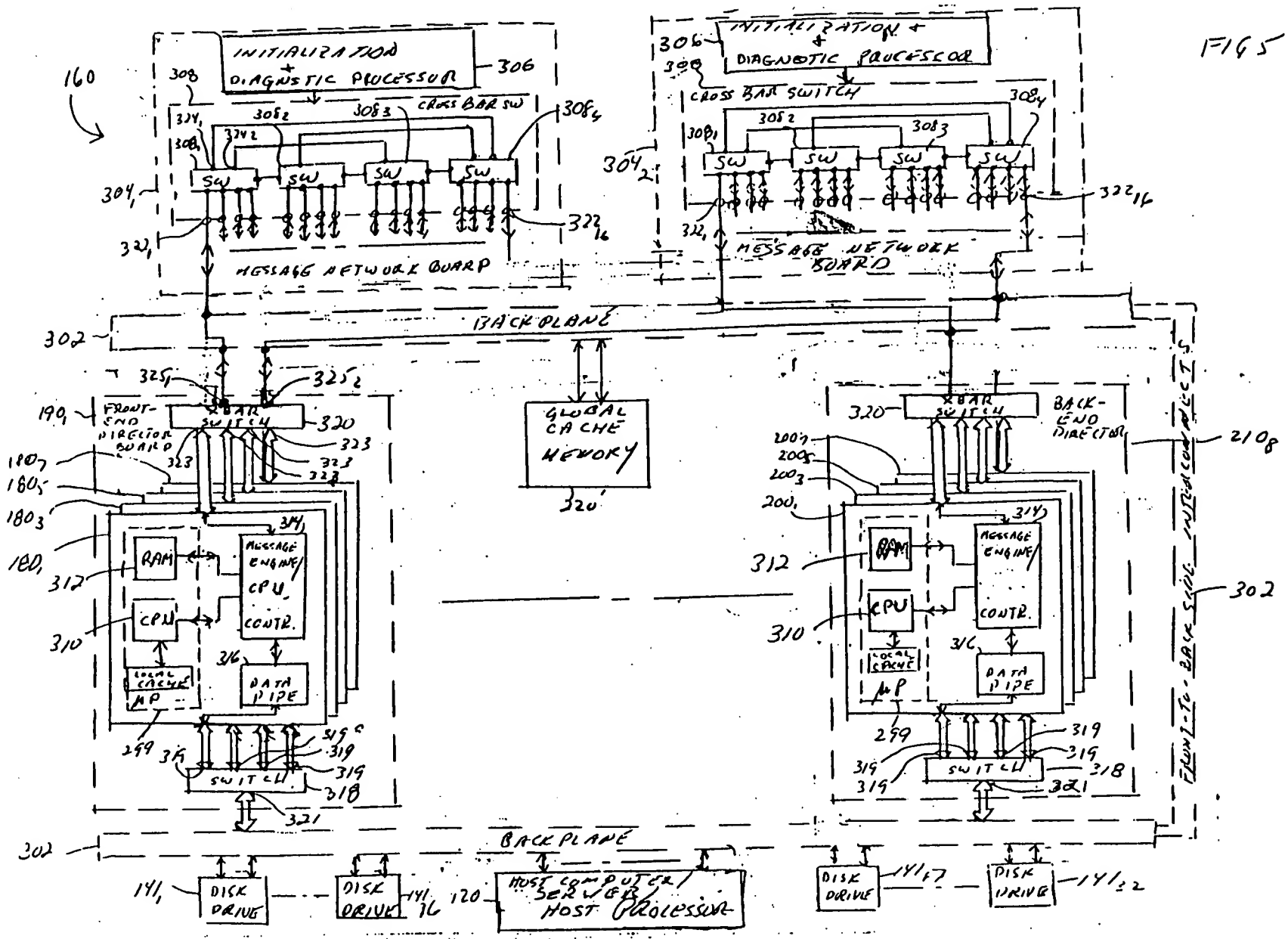

DIRECTOR BOARD

FIG. 3

FIG 4


CACHE MEMORY 220
MESSAGE NETWORK BOARD 304,
MESSAGE NETWORK BOARD 304 2
BACKPLANE 302
TO/FROM DISK DRIVES 140
TO/FROM HOST COMPUTER/ HOST PROCESSOR 120
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
BACKPLANE 302
CACHE MEMORY BOARD
CACHE MEMORY BOARD


160
INITIALIZATION + DIAGNOSTIC PROCESSOR
306
CROSS BAR SW
CROSS BAR SWITCH
SW
MESSAGE NETWORK BOARD
BACK PLANE
GLOBAL CACHE MEMORY
320'
FRONT-END DIRECTOR BOARD
BACK-END DIRECTOR
XBAR SWITCH
320
RAM
MESSAGE ENGINE/ CPU CONTR.
CPU
LOCAL CACHE MP
DATA PIPE
SWITCH
318
DISK DRIVE
HOST COMPUTER/ SERVER/ HOST PROCESSOR
120
FIG 5 - BACK SIDE INTERCONNECT

DOCKET 95555

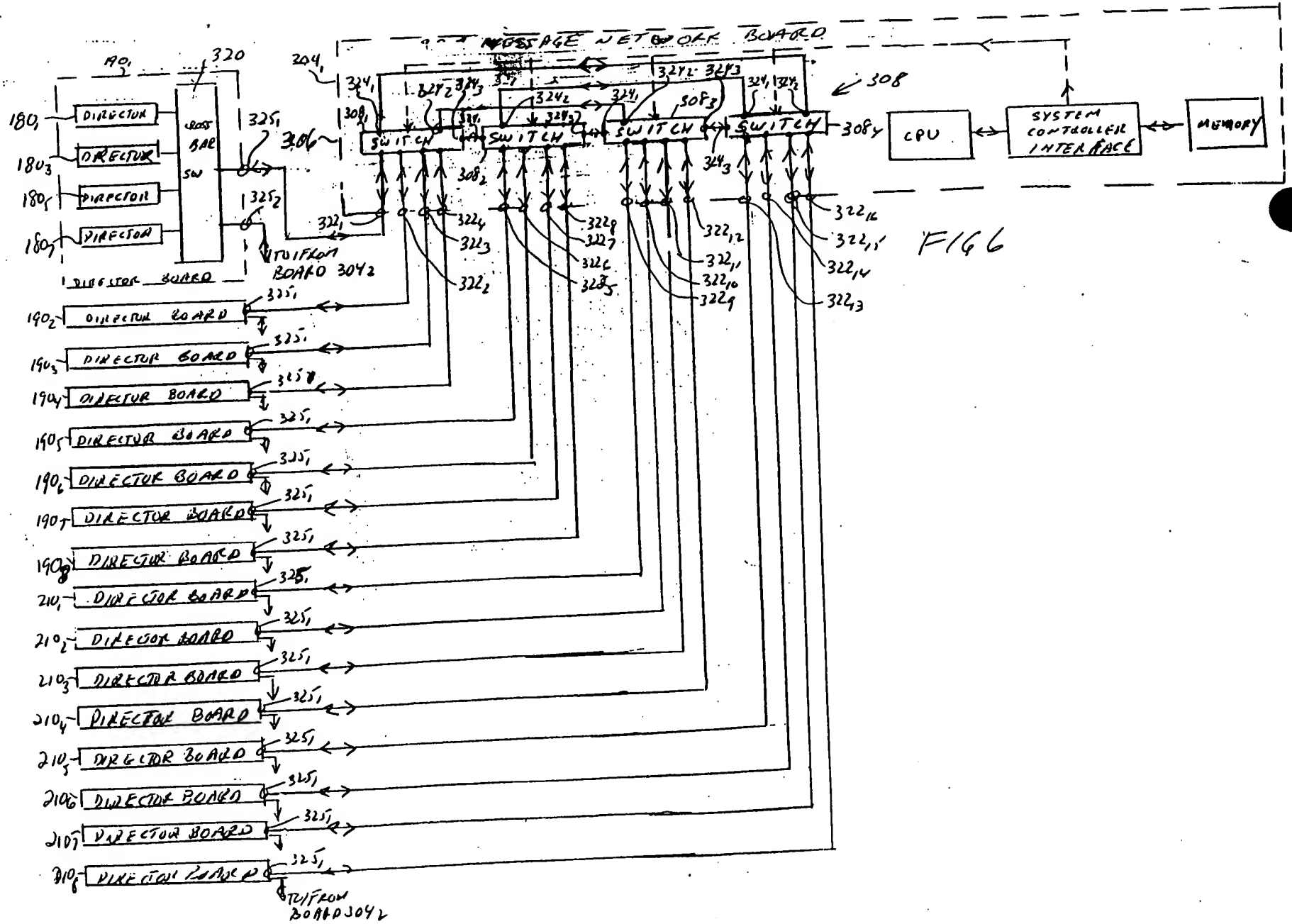
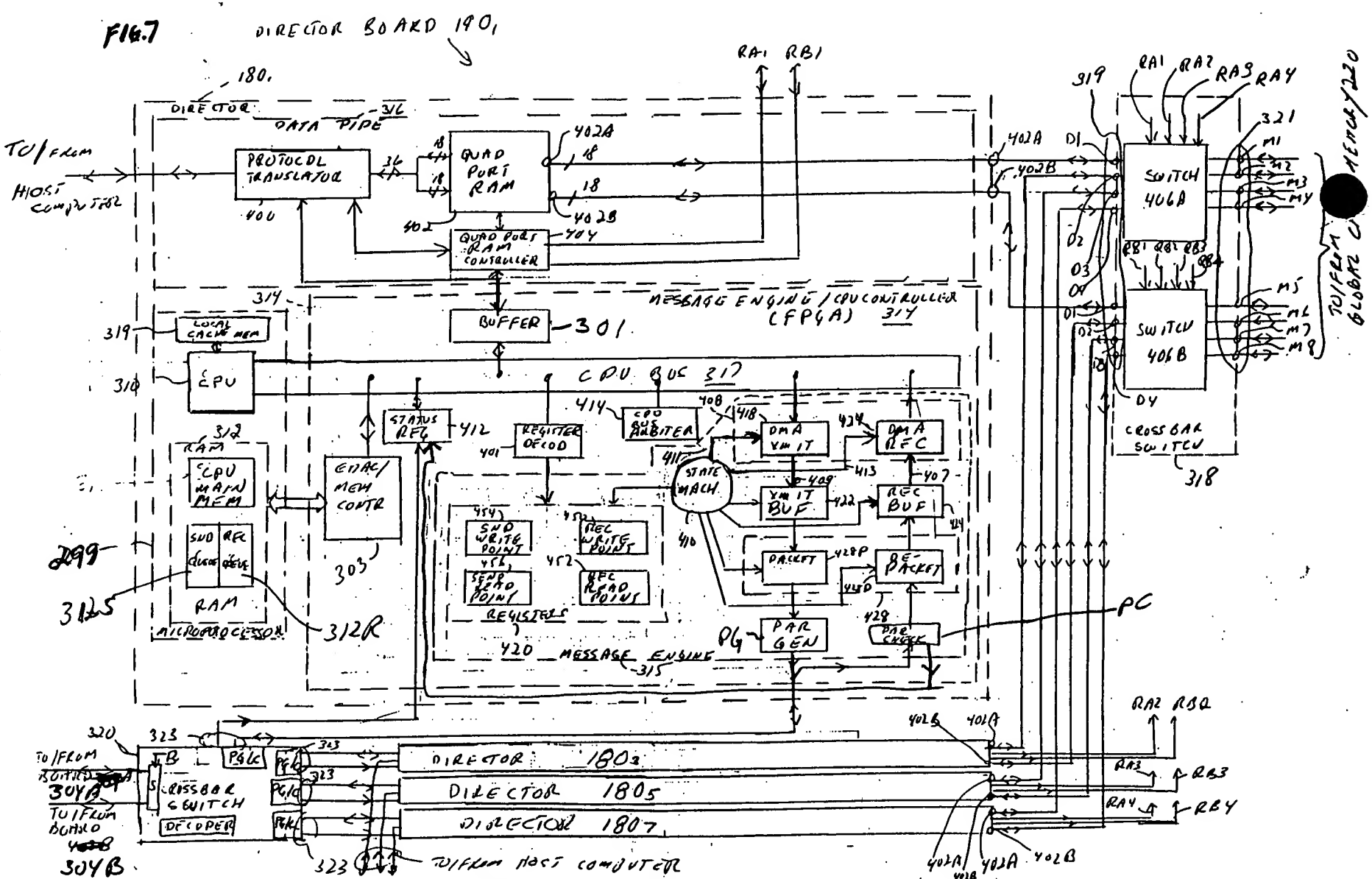


FIG 6

FIG. 7


DIRECTOR BOARD 190
180
DIRECTOR
DATA PIPE 316
TO/FROM HOST COMPUTER
PROTOCOL TRANSLATOR
400
QUAD PORT RAM
402
QUAD PORT RAM CONTROLLER
404
402A
402B
RA1 RB1
MESSAGE ENGINE / CPU CONTROLLER (FPGA) 314
BUFFER 301
LOCAL CACHE MEM
319
CPU
310
CPU BUS 317
RAM 312
CPU MAIN MEM
SND REC
RAM
312R
MICROPROCESSOR
299
312S
EDAC/ MEM CONTR
303
STATUS REG 412
REGISTER DECOD 401
CPU BUS ARBITER 414
STATE MACH 410
DMA XMIT 424
DMA REC 426
XMIT BUF 422
REC BUF 424
PACKET 428P
RE-PACKET 428
PAR GEN PG
PAR CHECK PC
SND WRITE POINT 454
REC WRITE POINT 452
SEND READ POINT 456
REC READ POINT 458
REGISTERS
420 MESSAGE ENGINE 315
SWITCH 406A
SWITCH 406B
CROSSBAR SWITCH 318
321
TO/FROM GLOBAL MEMORY 220
RA1 RA2 RA3 RA4
RB1 RB2 RB3 RB4
M1 M2 M3 M4
M5 M6 M7 M8
D1 D2 D3 D4
320
323
TO/FROM BOARD 304B
CROSSBAR SWITCH
DECODER
PG/C
DIRECTOR 1803
DIRECTOR 1805
DIRECTOR 1807
TO/FROM HOST COMPUTER
RA2 RB2
RA3 RB3
RA4 RB4

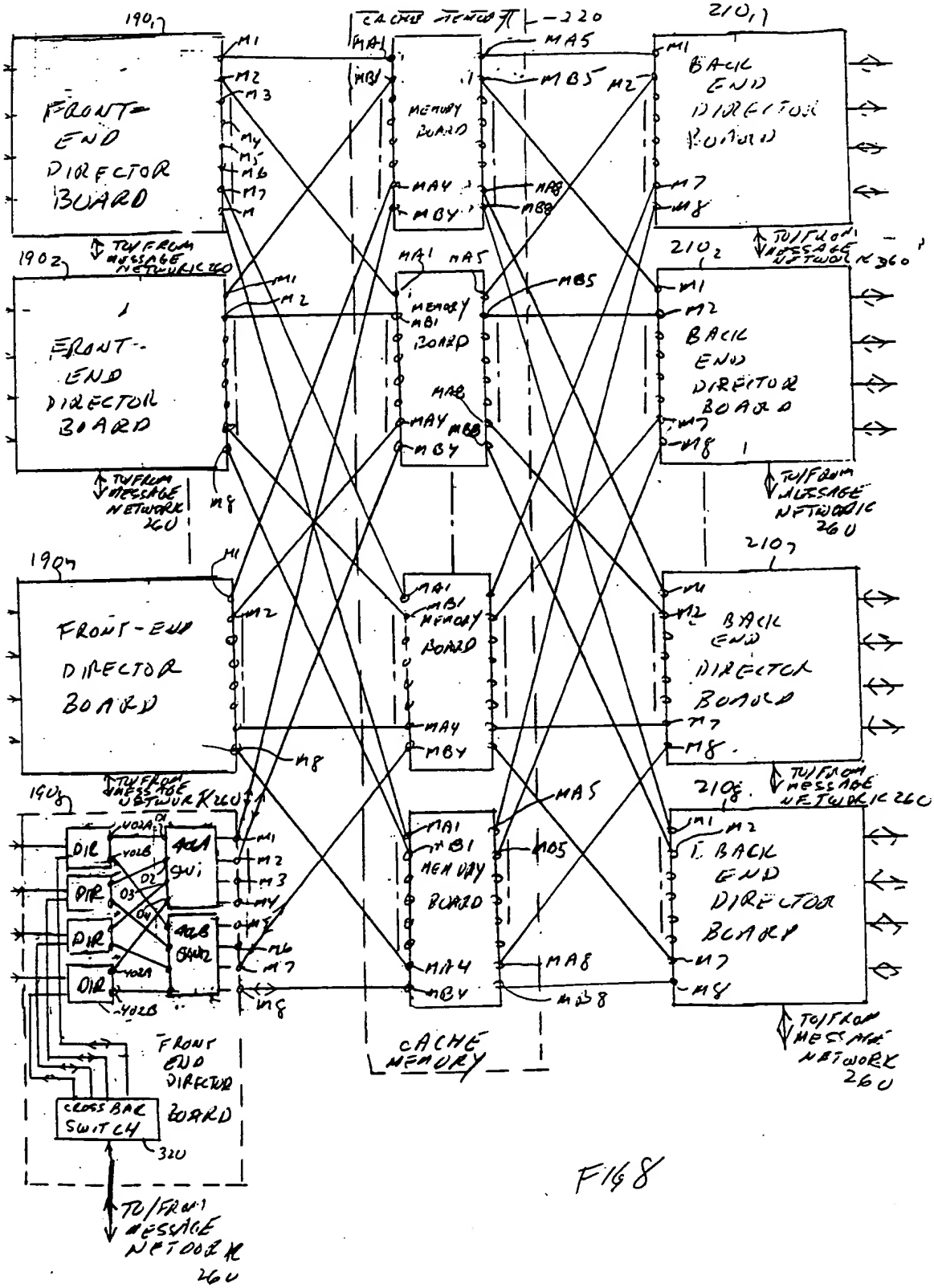
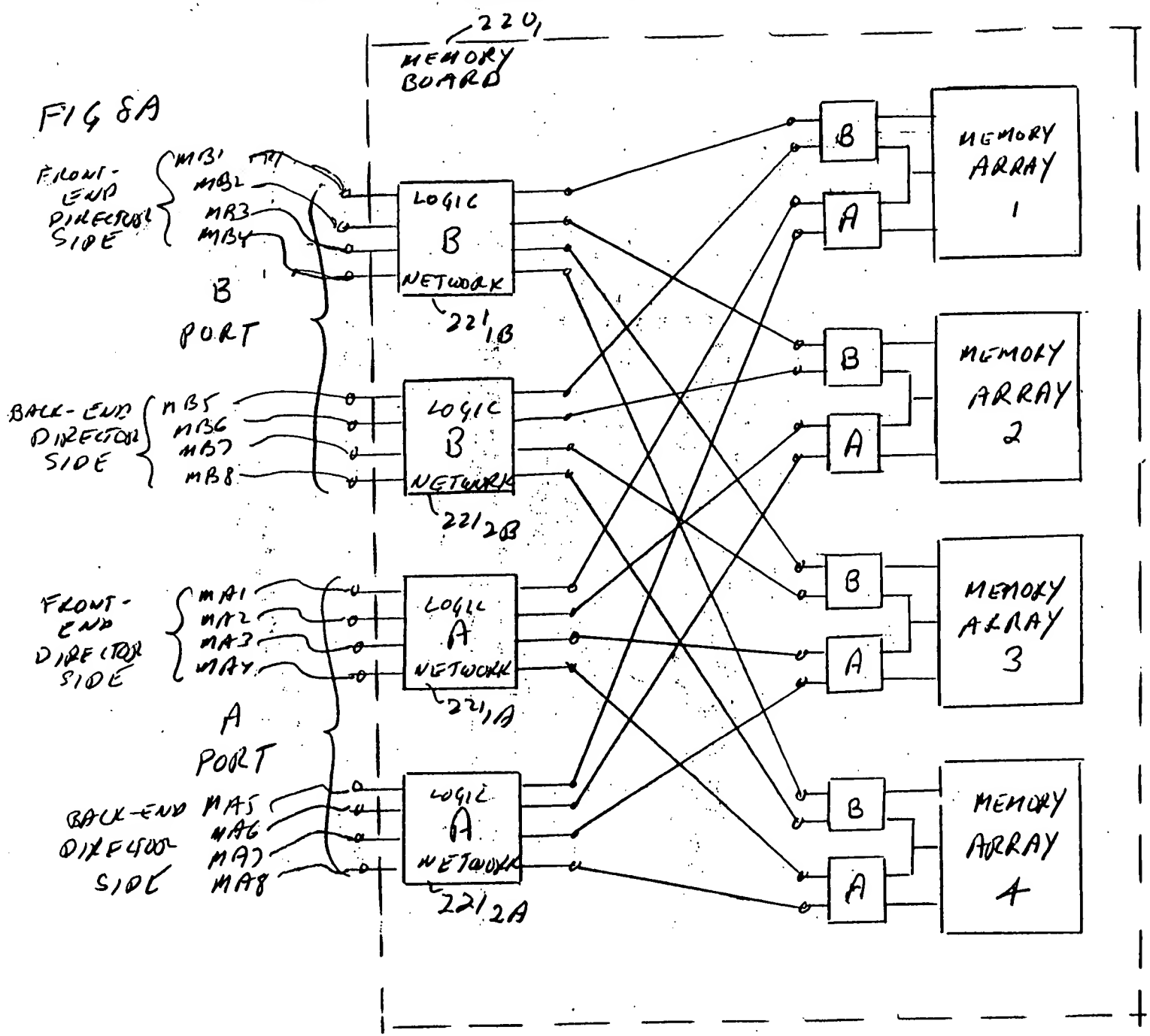

190,
FRONT-END DIRECTOR BOARD
190 2
FRONT-END DIRECTOR BOARD
190 7
FRONT-END DIRECTOR BOARD
190 8
FRONT END DIRECTOR BOARD
CROSS BAR SWITCH
320
TO/FROM MESSAGE NETWORK 260
CACHE MEMORY
220
MEMORY BOARD
MEMORY MB1 BOARD
MEM WAY BOARD
210,
BACK END DIRECTOR BOARD
210 2
BACK END DIRECTOR BOARD
210 7
BACK END DIRECTOR BOARD
210 8
BACK END DIRECTOR BOARD
TO/FROM MESSAGE NETWORK 260

FIG 8

EUROPEAN PATENT OFFICE

FIG 8A



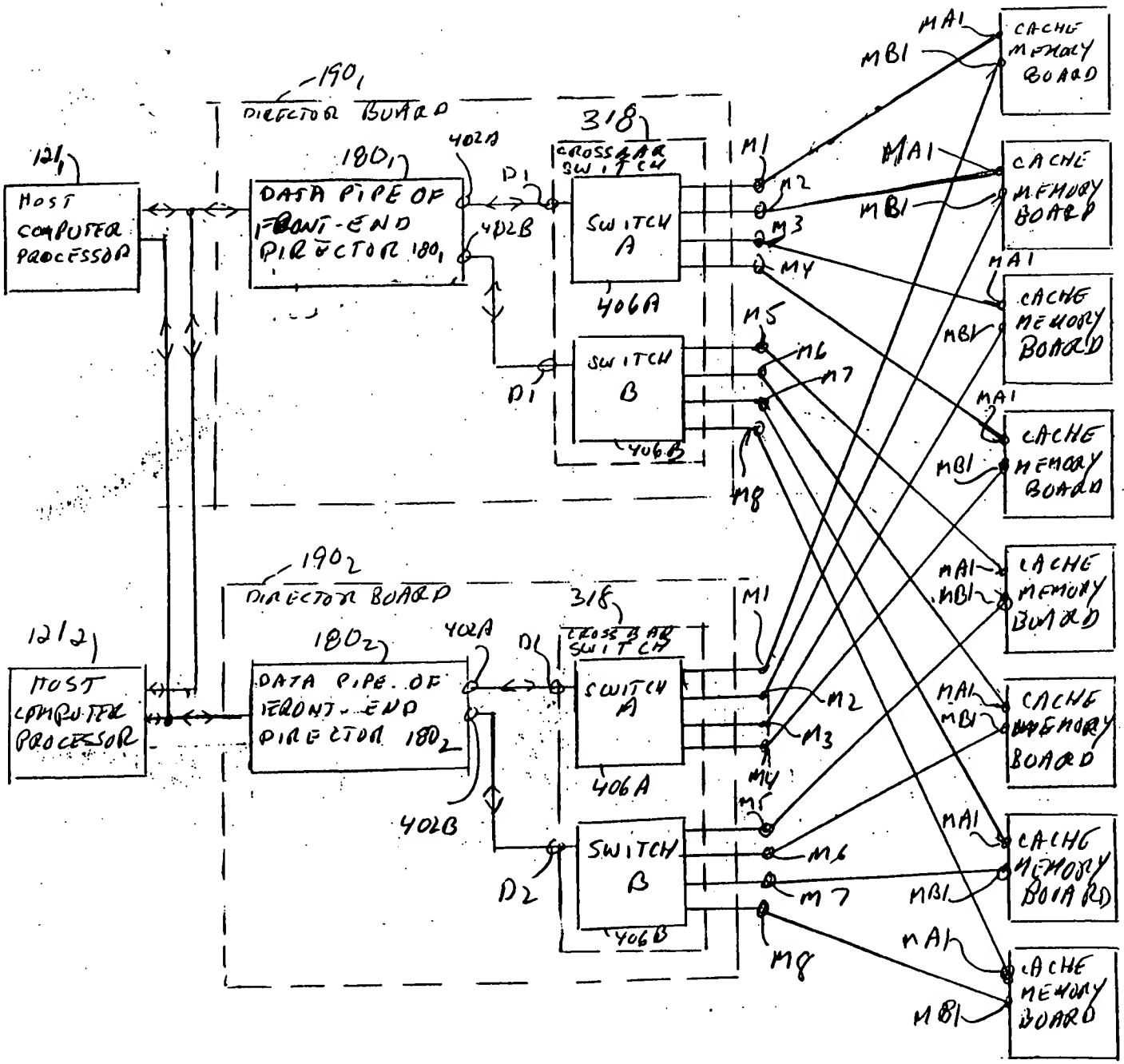

190₁
DIRECTOR BOARD
121₁
HOST COMPUTER PROCESSOR
180₁
DATA PIPE OF FRONT-END DIRECTOR 180₁
402A
402B
D1
318
CROSS-BAR SWITCH
SWITCH A
406A
SWITCH B
406B
M1
M2
M3
M4
M5
M6
M7
M8
MA1
MB1
CACHE MEMORY BOARD
190₂
DIRECTOR BOARD
121₂
HOST COMPUTER PROCESSOR
180₂
DATA PIPE OF FRONT-END DIRECTOR 180₂
D2

FIG 8B

FIG. 8C

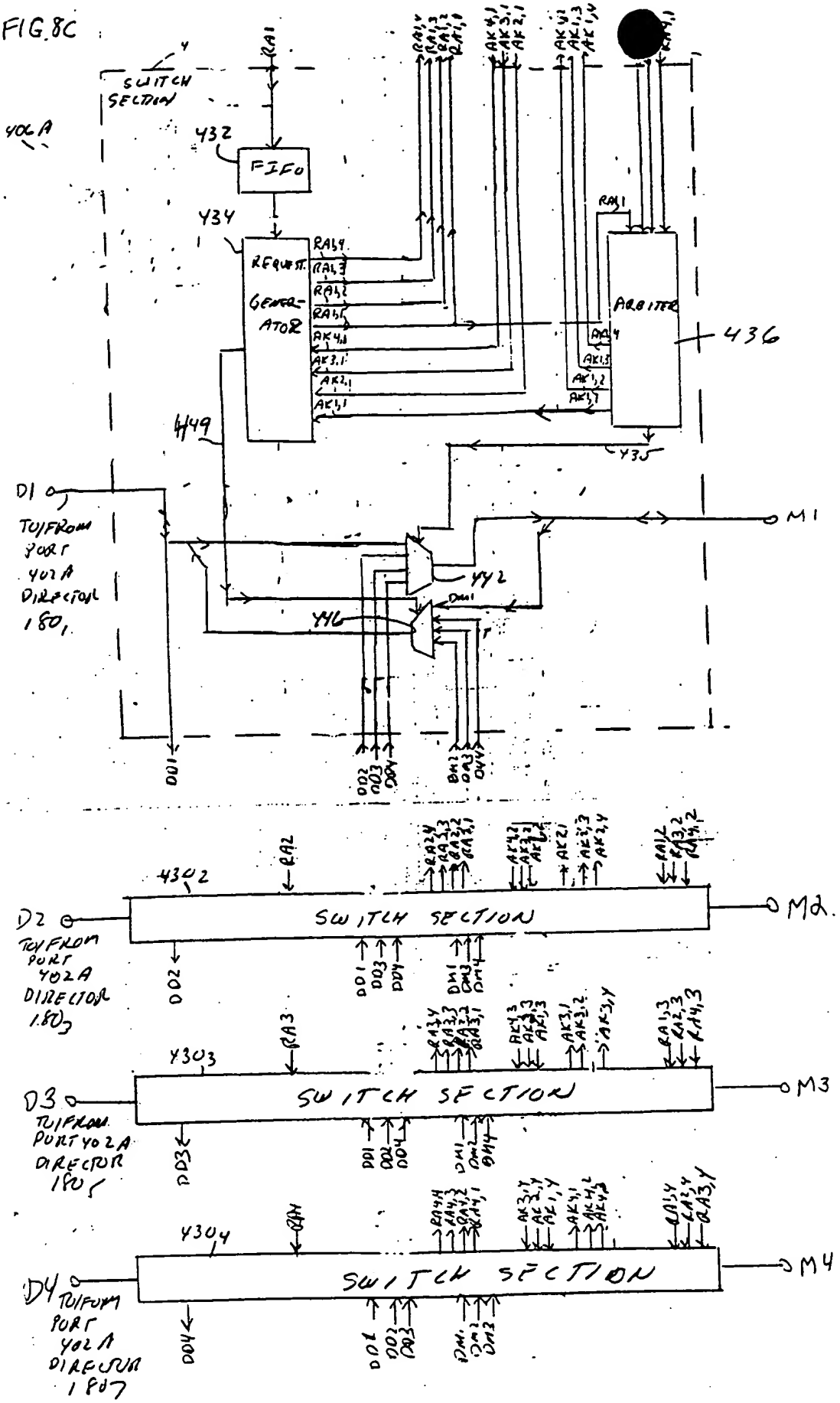

SWITCH SECTION
402A
432
FIFO
434
REQUEST GENERATOR
ARBITER
436
449
D1
TO/FROM PORT 402A DIRECTOR 180
M1
SWITCH SECTION
4302
D2
TO/FROM PORT 402A DIRECTOR 180
M2
4303
D3
TO/FROM PORT 402A DIRECTOR 180
M3
4304
D4
TO/FROM PORT 402A DIRECTOR 180
M4

FIG 9

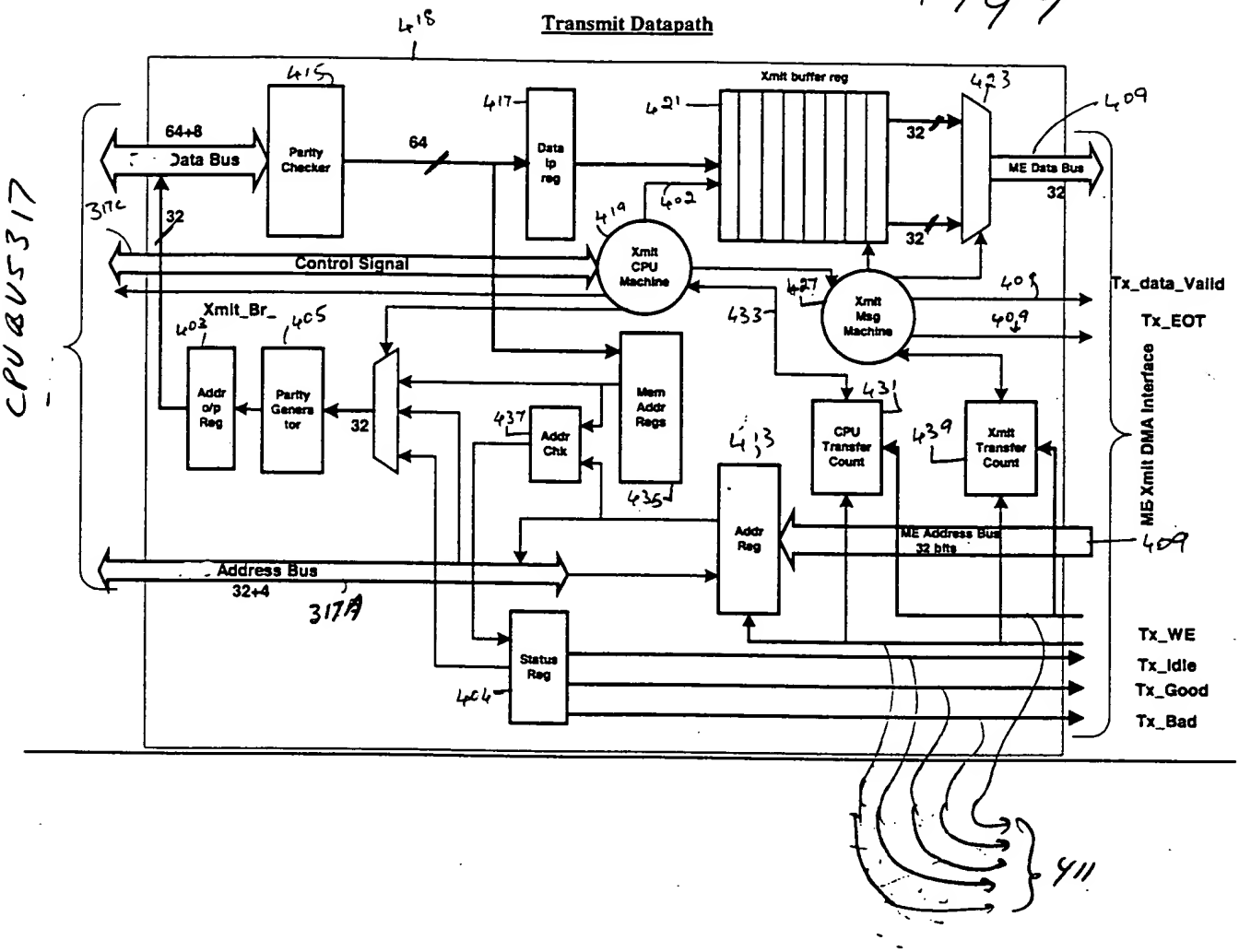
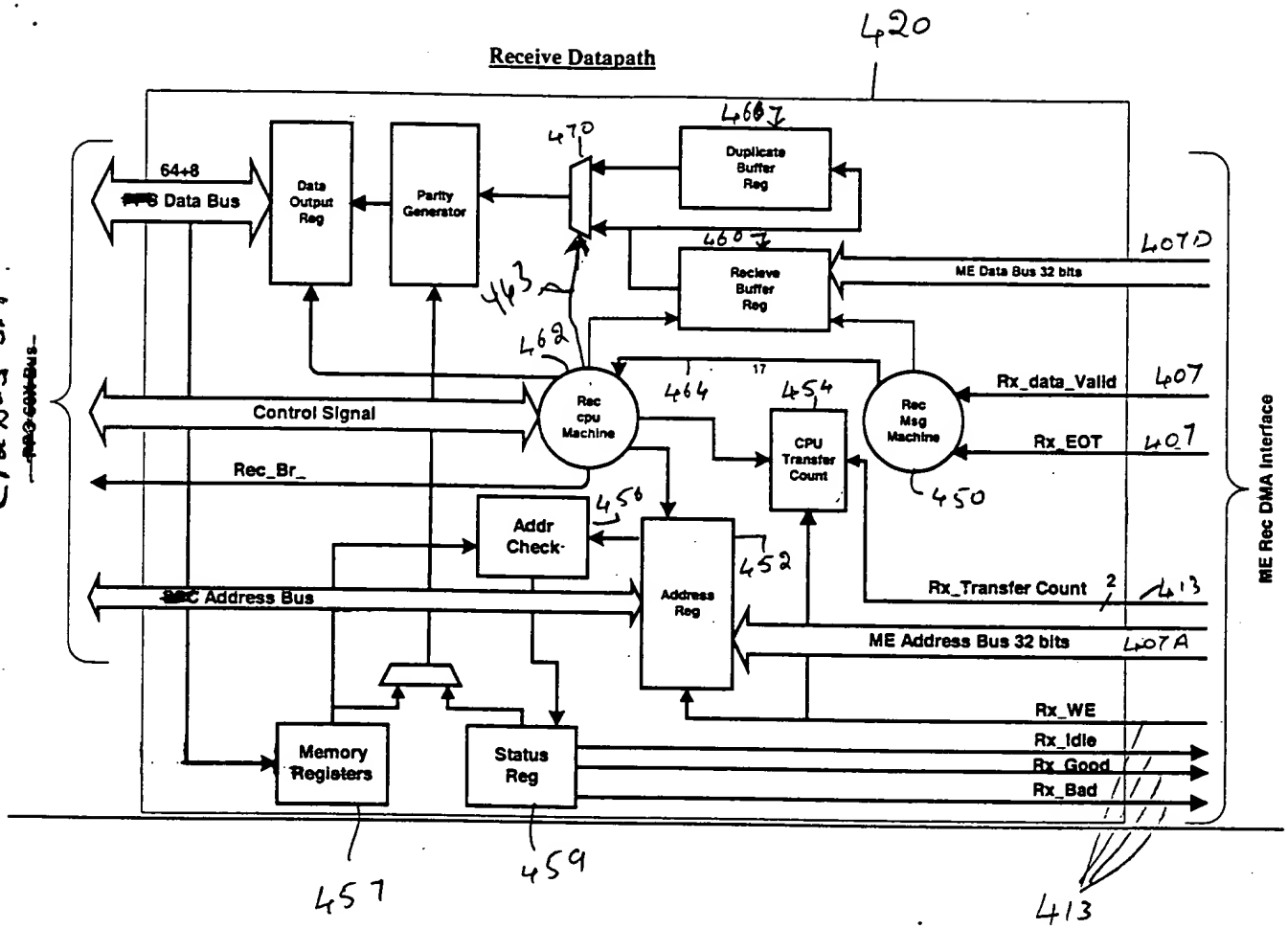

Transmit Datapath
418
415
417
421
423
409
64+8
Data Bus
Parity Checker
64
Data Ip reg
Xmit buffer reg
32
ME Data Bus
32
317c
32
419
402
Control Signal
Xmit CPU Machine
427
Xmit Msg Machine
409
Tx_data_Valid
Tx_EOT
433
Xmit_Br_
402
405
Addr o/p Reg
Parity Generator
32
Mem Addr Regs
437
Addr Chk
431
CPU Transfer Count
439
Xmit Transfer Count
413
435
Addr Reg
ME Address Bus 32 bits
409
ME Xmit DMA Interface
Address Bus
32+4
317A
Tx_WE
Tx_Idle
Tx_Good
Tx_Bad
Status Reg
404
411
CPU BUS 317

FIG 10


Receive Datapath
420
CPU BUS 317
64+8
Data Bus
Data Output Reg
Parity Generator
470
Duplicate Buffer Reg
460
Recieve Buffer Reg
ME Data Bus 32 bits
407D
463
462
Rec cpu Machine
464
17
454
CPU Transfer Count
Rec Msg Machine
Rx_data_Valid
407
Rx_EOT
407
450
Control Signal
Rec_Br_
456
Addr Check
452
Address Reg
Rec Address Bus
Rx_Transfer Count
2
413
ME Address Bus 32 bits
407A
Rx_WE
Rx_Idle
Rx_Good
Rx_Bad
Memory Registers
Status Reg
457
459
413
ME Rec DMA Interface

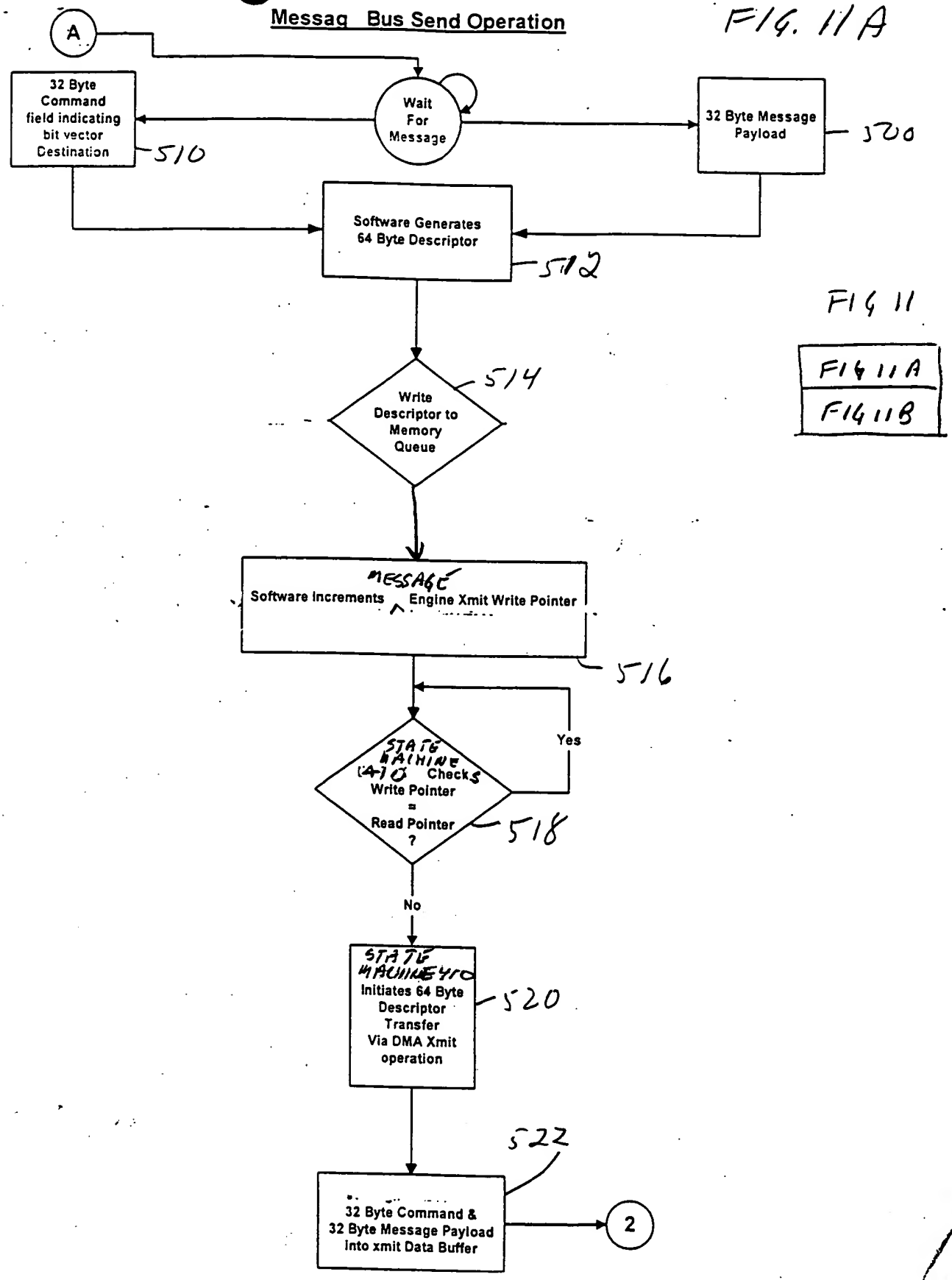


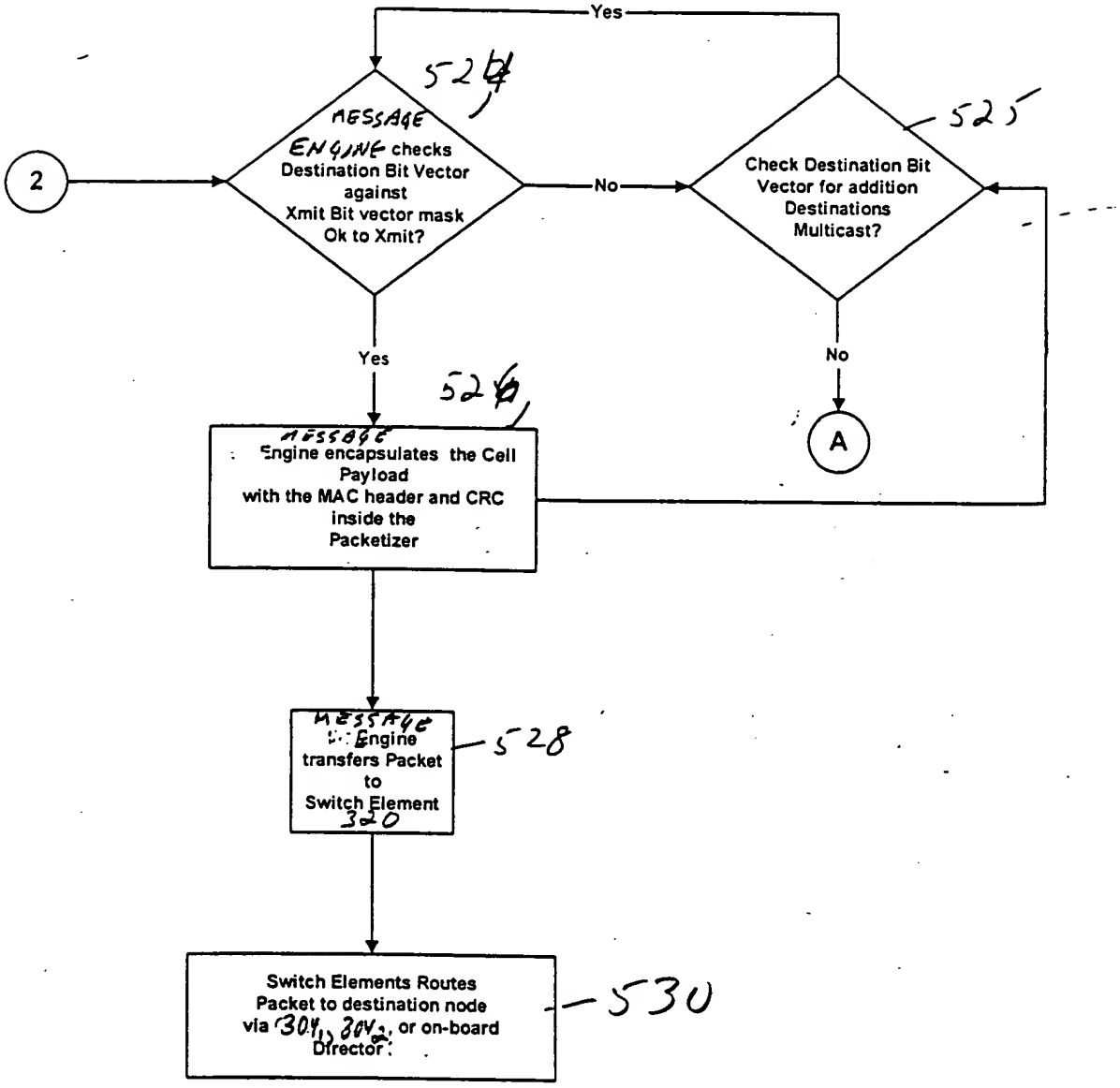
FIG. 11A

FIG 11

FIG 11A
FIG 11B

Message Bus Send Op ration Continued

FIG 11B



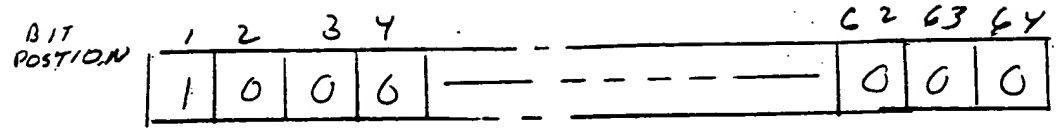


FIG 11C

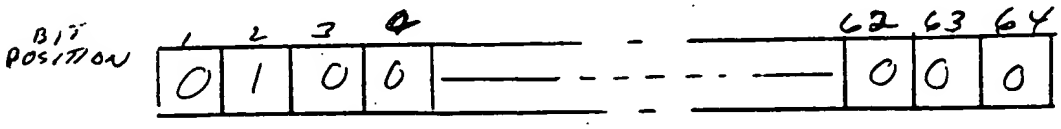


FIG 11D

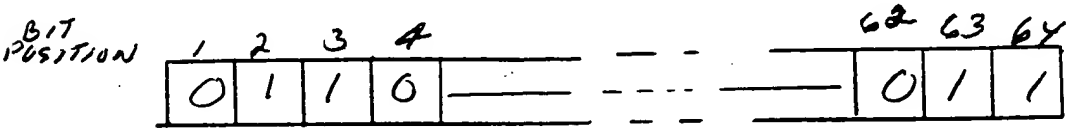


FIG 11E

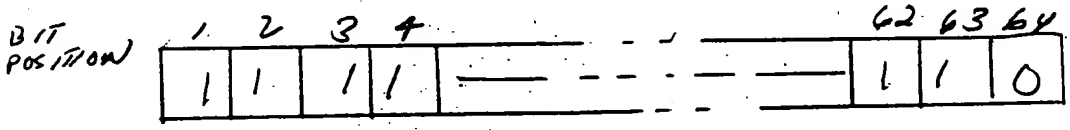


FIG 11F

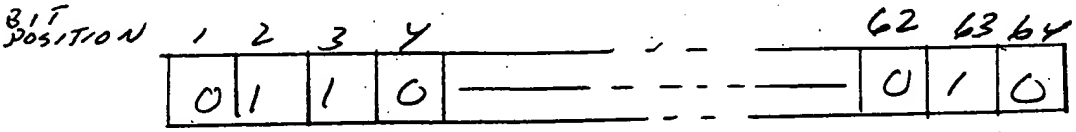


FIG 11G

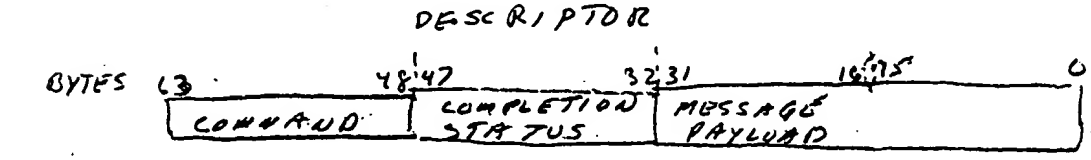


FIG 2A

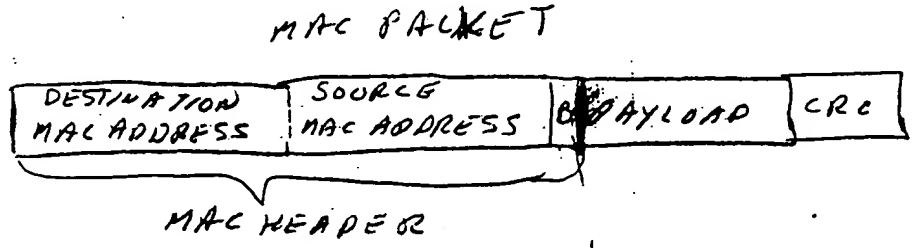


FIG 2B

M ssage Bus Receive Operation

FIG. 12A

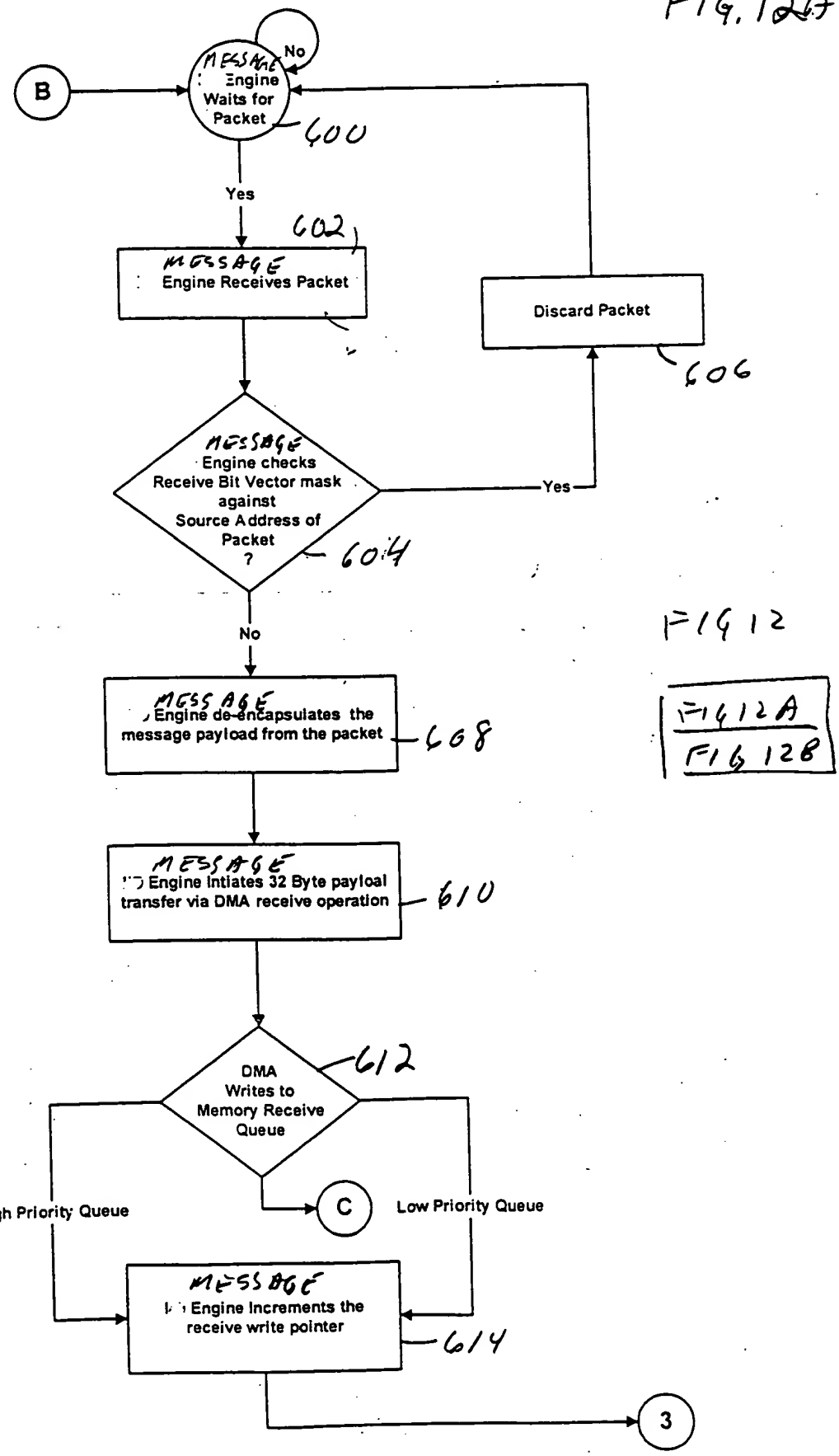


FIG 12

FIG 12A
FIG 12B

Message Bus Receive Operation Continued

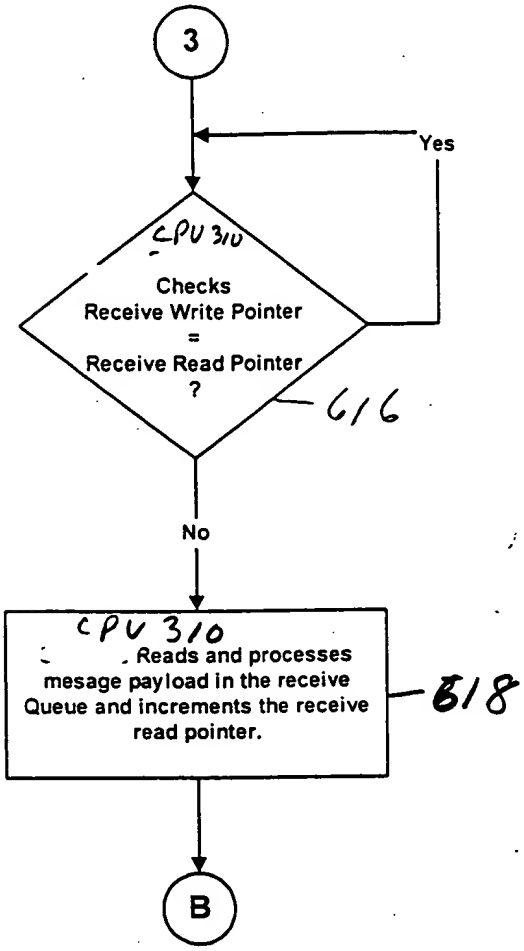


FIG 12B

Message Bus Acknowledgement Op ration

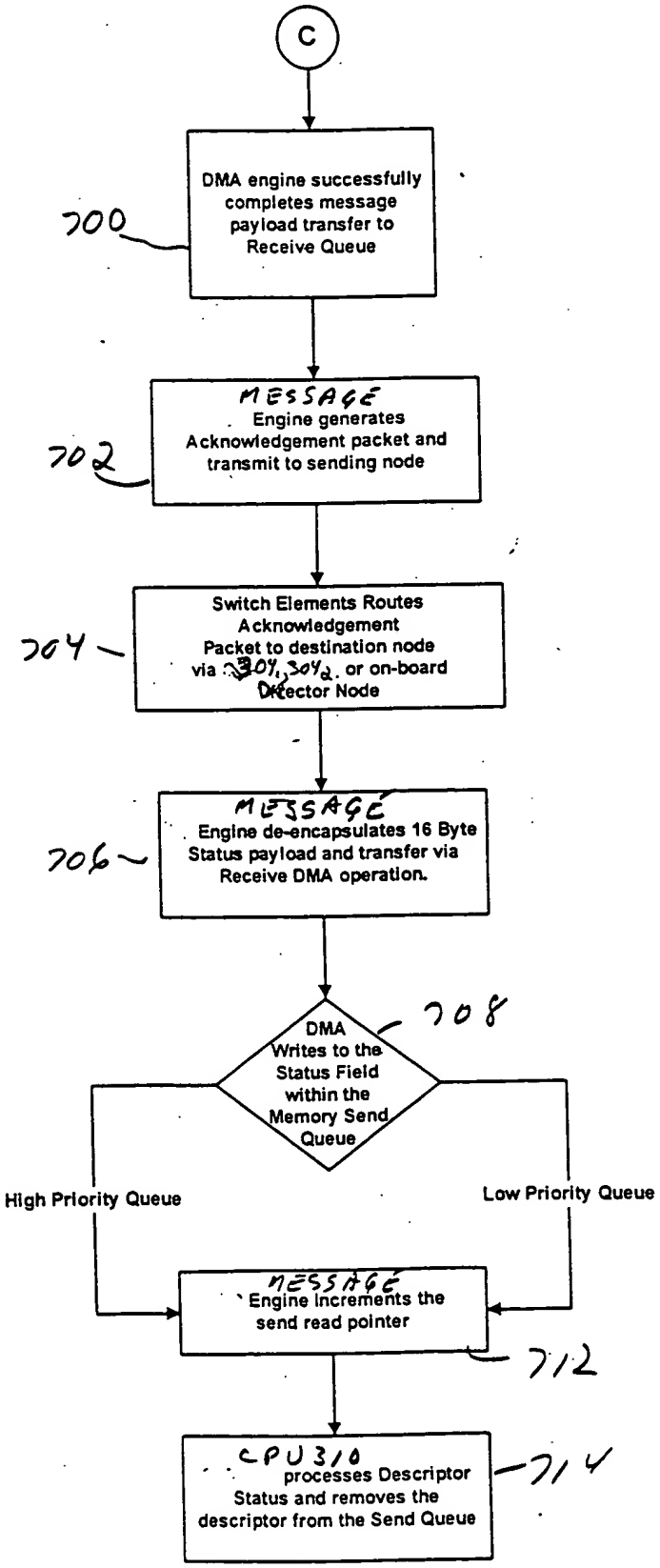
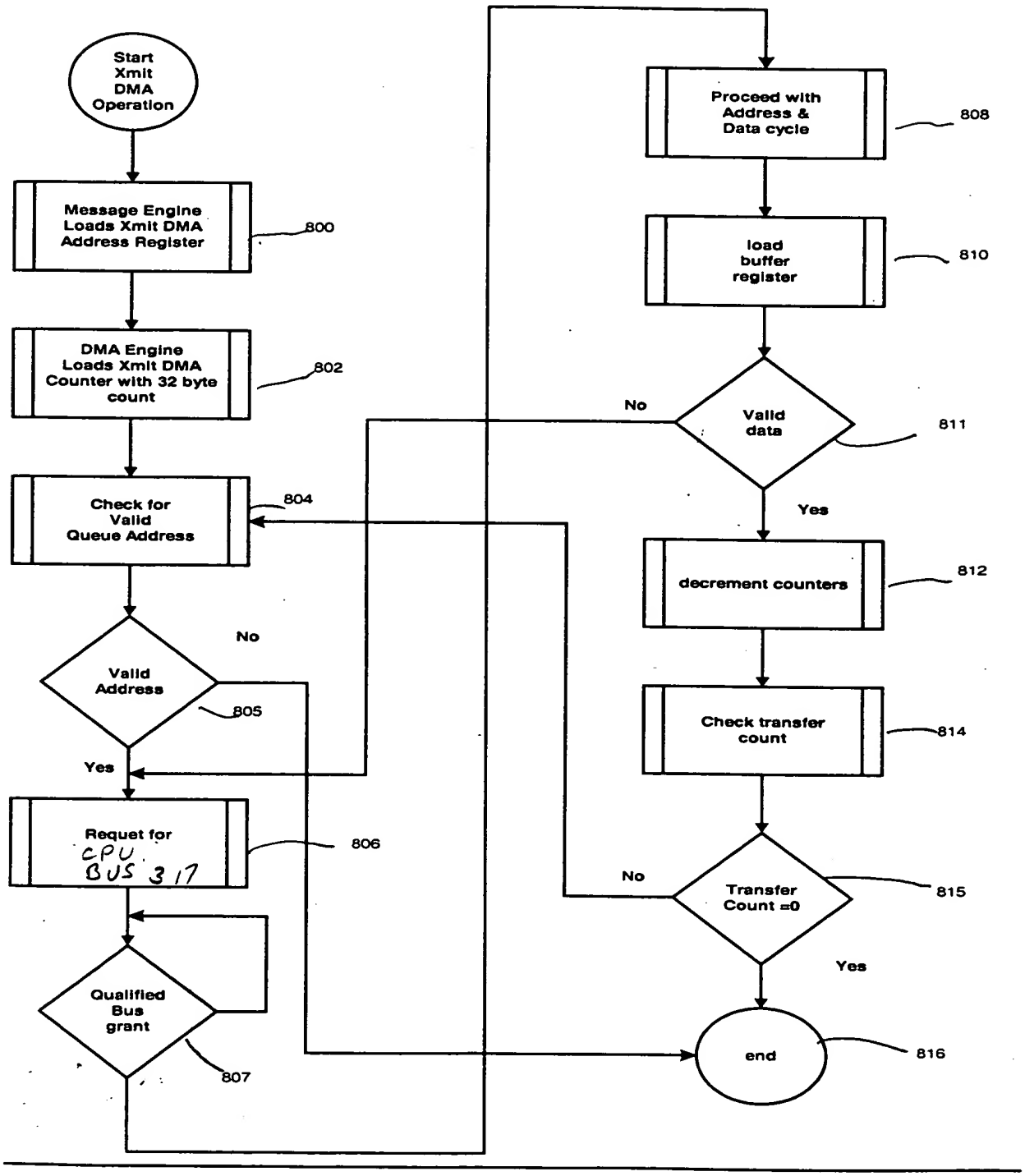


FIG. 13

FIG 14A

Xmit CPU flow



F-1414B

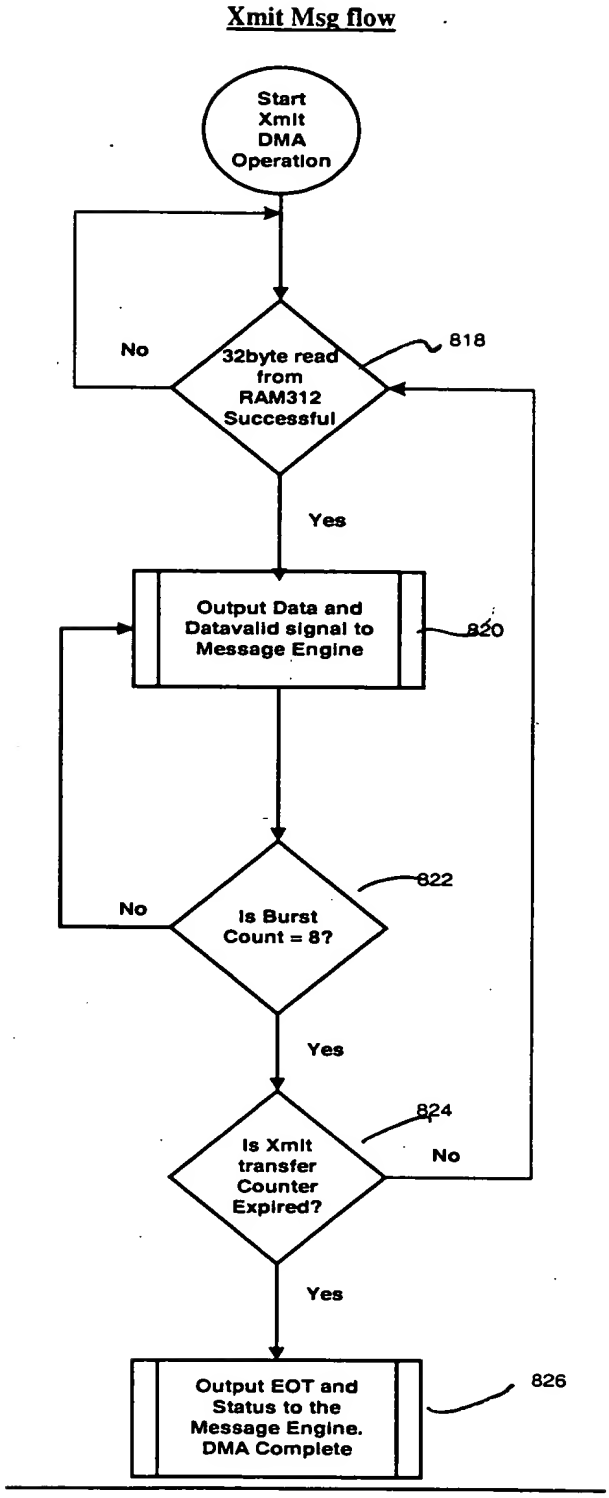

Xmit Msg flow
Start Xmit DMA Operation
32byte read from RAM312 Successful
818
No
Yes
Output Data and Datavalid signal to Message Engine
820
Is Burst Count = 8?
822
No
Yes
Is Xmit transfer Counter Expired?
824
No
Yes
Output EOT and Status to the Message Engine. DMA Complete
826

FIG 15A

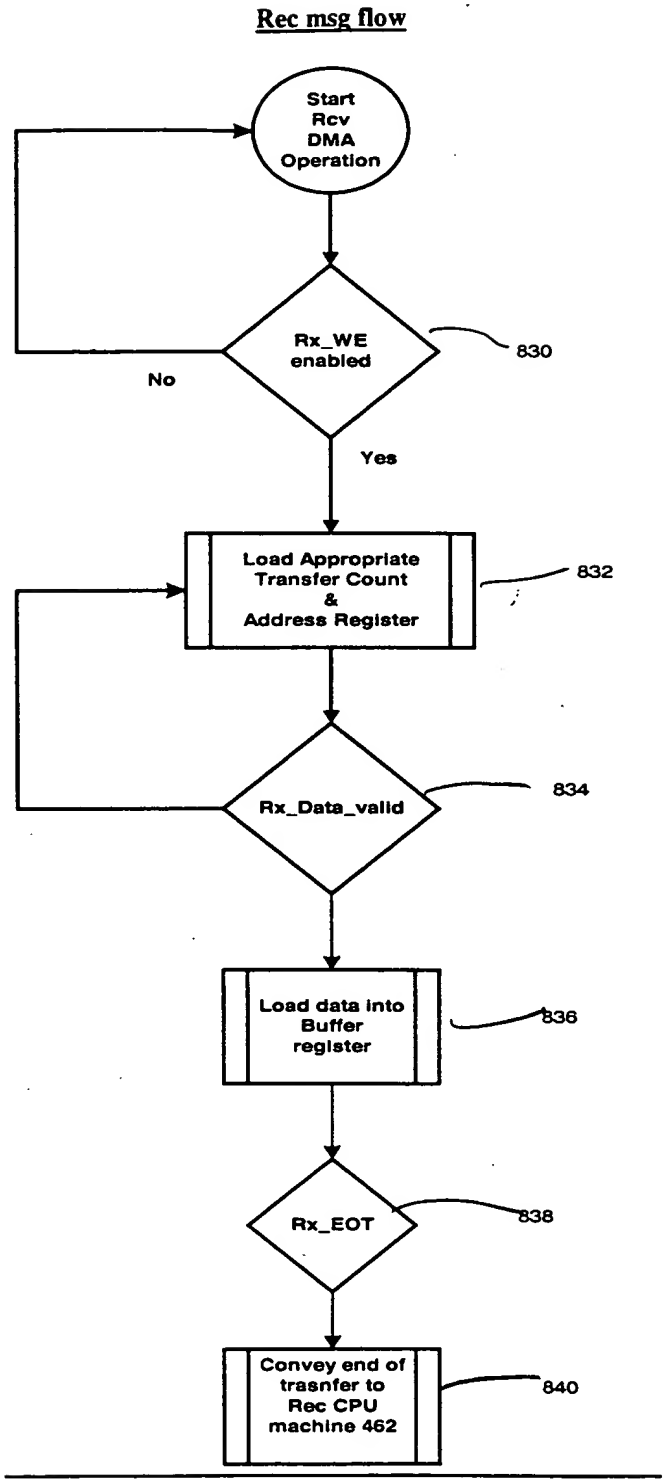
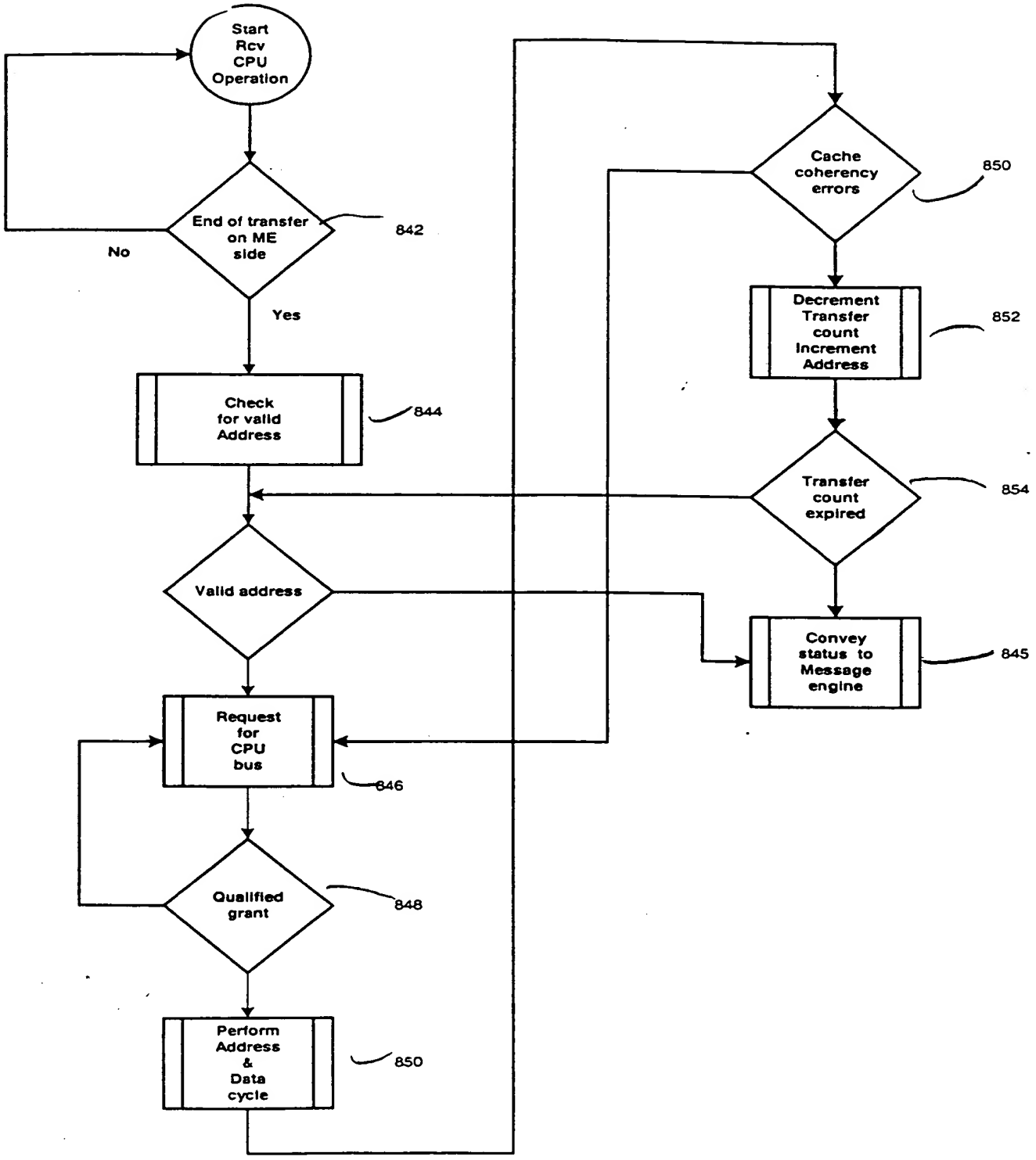

Rec msg flow
Start Rcv DMA Operation
Rx_WE enabled
830
No
Yes
Load Appropriate Transfer Count & Address Register
832
Rx_Data_valid
834
Load data into Buffer register
836
Rx_EOT
838
Convey end of trasnfer to Rec CPU machine 462
840

FIG 15B

Rec cpu flow